Response of the TeV BPM Upgrade Project to the Hardware Review
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Introduction:

On May 14, 2004 a review of the hardware design of the front end of the Tevatron BPM Upgrade Project was held. The reviewers included Brian Chase and Peter Prieto, and a written review was received from Brian Chase on May 19, 2004. This document is a response to that review and its recommendations.

Recommendation: *Remove the PLL and clock driver circuit from the timing card and put it in a 1 U rack chassis with a linear power supply. Add a low noise DDS clock to this chassis as an optional source to the VCO. Distribute the diagnostic signals from this chassis as well. As for the source of the diagnostic signal, you could use the high speed DAC signal from the timing card and distribute to all diagnostic cards with precision splitters. A wide band, white noise signal can be used to check the frequency response of the cables, filters and the system as a whole. Problems with converters or the data stream can also be diagnosed.*

Response: The project is designing the clock to perform better than the current EchoTek clock system, measured to be jitter of 15 ps. The PLL that will be used for the new clock circuit has a measured jitter of less than 3 ps. Our current estimate is that the total jitter of the system will be less than 10 ps. This represents 3 bits of information lost and is acceptable. The clock jitter that we have specified (15 ps) is more than adequate to achieve the precision and accuracy required by the upgraded system, as was shown with measurements with the current Recycler EchoTek board on Tevatron proton and antiproton beam. The clock driver signal has been checked and is compatible with the EchoTek.

The diagnostic signal will be transferred on the VME backplane. This is acceptable, given that the diagnostic signal is not a calibration so the signal quality is not of primary concern. The signal will be turned off when not in use and will therefore not produce noise on the VME backplane.

The question of diagnostics (the second part of the recommendation) is connected to the issue of relays and will be addressed when responding to the next recommendation.

Recommendation*: Remove the series relay and simplify the test modes to inject a signal or not. Even with just this relay, the termination impedance changes from 50 to 25 ohms when the relay closes. As far as board layout is concerned, all RF signals should be imbedded strip lines between ground planes. Pads and other component should be shielded if possible. Use shielded Mini-Circuit pads instead of resistors. Remember that 53 MHz is 21 times higher in frequency than the 2.5 MHz Recycler system so crosstalk is 21 times worse.*

Response: The series relays are part of the design of the diagnostics for this system. The design allows for direct injection of signal to the front-end of the EchoTek cards as well as injection of a signal through the BPM pickups in the tunnel. This capability will be very useful in debugging the system and is an important design consideration. We are aware of the drawbacks of using relays but believe that the benefit outweighs the concerns. A close look at a data sheet for one of the relays considered shows the impedance change to be small – on the order of 0.02% after >100,000 closings. This is acceptable. Test/prototype relays have been purchased and measurements will be made of their performance. The 25 ohm resistance is actually a design plus as it gives different level diagnostics signals for testing the system.

The board design will incorporate shielding. Signals are carried between ground planes and channels are isolated. Specifications on S11, S21 and S22 will be established. A prototype board will be obtained as soon as possible even if without filters so that these parameters can be measured in case iteration is required. These parameters will be measured as part of the acceptance of the production boards.

Other Concerns: *Drifts, calibrations, systematic errors, narrow band measurements.*

Responses: The precise techniques for measuring and controlling drifts are not all yet established but are part of the diagnostic and calibration systems being defined for the system. The goal is to achieve better than the specified values for accuracy and precision. Substantially better values may be possible with detailed offline analysis of the data (not part of the project).

The question of using an asynchronous clock to try to reduce systematic errors coming from the phase-locked clock system is one that the project will investigate. The design does allow for use of a synchronous clock.

Recommendation: *Provide a mode to make a pure narrow band measurement using 100 Hz BW filters on the I and Q data streams. Calculate positions to provide the required 100 Hz BW data. Filter the 100 Hz data down to 10 Hz for the required 10 Hz BW data. Use a low noise crystal 80 MHz clock source for measurement.*

Response: This may be a misunderstanding. Normal close orbit data is obtained with the EchoTek board filtering set to approximately 1 kHz bandwidth. Further averaging in the MVME processor can be used to average out synchrotron oscillations and to provide information at 10 Hz. No change to the current design is required.